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EXAMINER	
ALMEIDA, DEVIN E	

ART UNIT	PAPER NUMBER
2132	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/736,838	SON, HEE-KWAN	
	Examiner	Art Unit	
	DEVIN ALMEIDA	2132	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 January 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-53* is/are pending in the application.

4a) Of the above claim(s) *39-52* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-38 and 53* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

This action is in response to the papers filed 1/16/2008. In response to the restriction requirement applicant elects with traverse to claims 1-38 and 53 were received for consideration.

Response to Arguments

Applicant's arguments have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1- 21, 24-38 and 53 are rejected under 35 U.S.C. 102(b) as being anticipated by Essig et al (U.S. 4,646,257). With respect to claim 1, a booth processor, comprising: a booth recoder (see figure 1 element 161 and figure 3 element 217 column 5 lines 1-50); and a booth register, wherein an input to the booth register is at least one output from the booth recoder (see figure 1 element 119 and column 5 lines 1-50).

With respect to claim 2, wherein the booth register is a feedback register that stores at least one output value of the booth recoder to be fed back to the booth recoder (see figure 1 element 119 and column 5 lines 1-50).

With respect to claim 3, wherein the output value is a partial product selection signal, where the partial product selection signal is used to select a partial product value (see figure 3).

With respect to claim 4, wherein the booth register is a pipeline register, the pipeline register stores output values of the booth recoder (see figure 1 and 3).

With respect to claim 5, a modulus processor, comprising: a modulus recoder (see figure 1 element 111); and a modulus feedback register, wherein an input to the feedback register is at least one output from the modulus recoder (see figure 1 element 147).

With respect to claim 6, wherein the modulus feedback register stores at least one output value of the modulus recoder to be fed back to the modulus recoder (see figure 1 element 14).

With respect to claim 7, wherein the output value is a multiple modulus selection signal, where the multiple modulus selection signal is used to select a multiple modulus value (see column 3 line 9 – 66).

With respect to claim 8, a multiplier, comprising: a booth recoder (see figure 1 element 161 and figure 3 element 217 column 5 lines 1-50); a partial product synch register, wherein an input to the partial product synch register is at least one output from the booth recoder (see figure 3); a modulus recoder (see figure 1 element 111); and a

multiple modulus synch register, wherein an input to the multiple modulus synch register is at least one output from the modulus recoder (see figure 1 element 147), where the partial product synch register and the multiple modulus synch register are used to synchronize signals derived from the outputs of the booth recoder and the modulus recoder (see column 3 line 9 – 66 and column 5 lines 1-50).

With respect to claim 9, further comprising: a booth AND gate, wherein at least one value from the partial product synch register is input to the booth AND gate (see figure 1).

With respect to claim 10, further comprising: a modulus AND gate, wherein at least one value from the multiple modulus synch register is input to the modulus AND gate (see figure 1).

With respect to claim 11, a multiplier, comprising: a modulus recoder (see figure 1 element 111); a modulus feedback register, wherein an input to the modulus feedback register is at least one output from the modulus recoder (see figure 1 element 14); a booth recoder (see figure 1 element 161 and figure 3 element 217 column 5 lines 1-50); and a booth register, wherein an input to the booth register is at least one output from the booth recoder (see figure 1 element 119 and column 5 lines 1-50), where the modulus feedback register and the booth register save values enabling decreased computation power usage in the multiplier (see column 3 line 9 – 66 and column 5 lines 1-50).

With respect to claim 12, wherein the booth register is a feedback register that stores at least one output value of the booth recoder to be fed back to the booth recoder (see figure 1 element 119 and column 5 lines 1-50).

With respect to claim 13, wherein the output value is a partial product selection signal, where the partial product selection signal is used to select a partial product value (see figure 3).

With respect to claim 14, wherein the booth register is a pipeline register, the pipeline register stores output values of the booth recoder (see figure 1 and 3).

With respect to claim 15, wherein the modulus feedback register stores at least one output value of the modulus recoder to be fed back to the modulus recoder (see figure 1 element 14).

With respect to claim 16, wherein the output value is a multiple modulus selection signal, where the multiple modulus selection signal is used to select a multiple modulus value (see column 3 line 9 – 66).

With respect to claim 17, further comprising: a booth AND gate, wherein at least one value from the booth register is input to the booth AND gate (see figure 1).

With respect to claim 18, further comprising: a modulus AND gate, wherein at least one value from the modulus feedback register is input to the modulus AND gate (see figure 1).

With respect to claim 19, a partial product generator (see figure 1B), comprising: a booth recoder (see figure 1 element 161 and figure 3 element 217 column 5 lines 1-50); and a mux (see figure 1), wherein the mux inputs at least one output from the booth

recoder, where the booth recoder and the mux are used to obtain a partial product (see figure 1).

With respect to claim 20. The partial product generator of claim 19, further comprising: a booth AND gate (see figure 1), wherein at least one value from the mux is input to the booth AND gate (see figure 1B).

With respect to claim 21, wherein the booth recoder generates a partial product selection signal and a bit pattern is assigned to any value of the partial product selection signal that is prohibited based on a previous value of the partial product selection signal (see figure 3).

With respect to claim 24, wherein the booth recoder further comprises: a first mux, wherein the first mux inputs (see figure 1 element 159) a first portion of the previous value of the partial product selection signal and outputs a first portion of a current partial product selection signal; and a second mux, wherein the second mux inputs (see figure 1 element 157) a second portion of the previous value of the partial product selection signal and outputs a second portion of a current partial product selection signal (see column 3 line 9 – 66 and column 5 lines 1-50).

With respect to claim 25, wherein the first mux and the second mux are 8:1 muxs (see figure 1).

With respect to claim 26, a multiple modulus generator, comprising: a modulus recoder (see figure 1 element 111); and a mux (see figure 1 element 145), wherein the modulus recoder generates a current multiple modulus selection signal unless an enabling signal has a predetermined value, if the enabling signal has a predetermined

value, a previous value of the selection signal is used without generating a multiple modulus selection signal, the selection signal is used to select a multiple modulus value (see column 3 line 9 – 66 and column 5 lines 1-50).

With respect to claim 27, further comprising: a modulus AND gate, wherein at least one value from the mux is input to the modulus AND gate (see figure 1).

With respect to claim 28, wherein the modulus recoder further comprises: a first mux (see figure 1 element 159), wherein the first mux inputs a first portion of the previous value of the selection signal and outputs a first portion of a current multiple modulus selection signal; and a second mux (see figure 1 element 157), wherein the second mux inputs a second portion of the previous value of the selection signal and outputs a second portion of a current multiple modulus selection signal (see column 3 line 9 – 66 and column 5 lines 1-50).

With respect to claim 29. The multiple modulus generator of claim 28, wherein the first mux and the second mux are 8:1 muxs (see figure 1).

With respect to claim 30, a multiplier, comprising: a modulus recoder (see figure 1 element 111); a modulus feedback register, wherein an input to the modulus feedback register is at least one output from the modulus recoder (see figure 1 element 147); a modulus synch register, wherein an input to the modulus synch register is at least one output from the modulus recoder (see figure 1 element 153); a booth recoder (see figure 1 element 161 and figure 3 element 217 column 5 lines 1-50); a booth synch register, wherein an input to the booth synch register is at least one output from the booth recoder (see figure 1 element 119 and column 5 lines 1-50); and a booth register,

wherein an input to the booth register is at least one output from the booth recoder (see figure 1 element 119 and column 5 lines 1-50), where the modulus feedback register and the booth register save values enabling decreased computation power usage in the multiplier, and where the booth synch register and the modulus synch register are used to synchronize signals derived from the outputs of the booth recoder and the modulus recoder to decrease glitches (see column 3 line 9 – 66 and column 5 lines 1-50).

With respect to claim 31, wherein the booth register is a feedback register that stores at least one output value of the booth recoder to be fed back to the booth recoder (see figure 1 element 119 and column 5 lines 1-50).

With respect to claim 32, wherein the output value is a partial product selection signal, where the partial product selection signal is used to select a partial product value (see figure 3).

With respect to claim 33, wherein the booth register is a pipeline register, the pipeline register stores output values of the booth recoder (see figure 1 and 3).

With respect to claim 34, wherein the modulus feedback register stores at least one output value of the modulus recoder to be fed back to the modulus recoder (see figure 1 element 14).

With respect to claim 35, wherein the output value is a multiple modulus selection signal, where the multiple modulus selection signal is used to select a multiple modulus value (see column 3 line 9 – 66).

With respect to claim 36, further comprising: a booth AND gate, wherein at least one value from the booth sync register is input to the booth AND gate (see figure 1).

With respect to claim 37, further comprising: a modulus AND gate, wherein at least one value from the modulus syncregister is input to the modulus AND gate (see figure 1).

With respect to claim 38, wherein a multiple modulus value and a partial product value are synchronized by using values from the modulus synch register and values from the booth synch register (see column 3 line 9 – 66 and column 5 lines 1-50).

With respect to claim 53, a Montgomery multiplier comprising; means for inputting, wherein the means for input, enters the values for a modulus, multiplicand, and a multiplier (see abstract); means for booth storing, wherein the means for booth storing stores at least one output value from a booth recoder (see figure 1 element 161 and figure 3 element 217 column 5 lines 1-50); means for modulus storing, wherein the means for modulus storing stores at least one output value from a modulus recoder (see figure 1 element 111); means for partial product generation, wherein the means for partial product generation produces a partial product value using the input from the means for input (see figure 3); means for multiple modulus generation, wherein the means for multiple modulus generation produces a multiple modulus value using the input from the means for input (see figure 1); means for synchronizing, wherein the means for synchronizing synchronizes the partial product value and the multiple modulus value (see column 3 line 9 – 66 and column 5 lines 1-50); and means for accumulating, wherein the means for accumulating inputs the synchronized partial product value and the multiple modulus value and produces a result for the Montgomery multiplier (see column 3 line 9 – 66 and column 5 lines 1-50).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 22 and 23 rejected under 35 U.S.C. 103(a) as being unpatentable over Essig et al (U.S. 4,646,257) in view of Takano et al (US 5,790,874). Abbott teaches everything with respect to claim 21 above but does not teach with respect to claim 22, wherein the bit pattern is chosen so that the hamming distance between the current value of the partial product selection signal and the previous value of the partial product selection signal is reduced. Takano teach with respect to claim 22, wherein the bit pattern is chosen so that the hamming distance between the current value of the partial product selection signal and the previous value of the partial product selection signal is reduced (see Abstract). It would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains to have reduced the hamming distance to reduce the power consumption needed to perform the action (see Abstract). Therefore one would have been motivated to have reduced the hamming distance between bit sequences.

With respect to claim 23. The partial product generator of claim 21, wherein the bit pattern is chosen so that the average temporal hamming distance between the

current value of the partial product selection signals and their corresponding previous values are reduced (see Adstract).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Devin Almeida whose telephone number is 571-270-1018. The examiner can normally be reached on Monday-Thursday from 7:30 A.M. to 5:00 P.M. The examiner can also be reached on alternate Fridays from 7:30 A.M. to 4:00 P.M.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Gilberto Barron, can be reached on 571-272-3799. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Devin Almeida
Patent Examiner
4/15/2008

/Benjamin E Lanier/
Primary Examiner, Art Unit 2132